Paralleling Power MOSFETs

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Whenever devices are operated in parallel, due consideration should be given to the sharing between devices to ensure that the individual units are operated within their limits. Items that must be considered to successfully parallel MOSFETs are: gate circuitry, layout considerations, current unbalance, and temperature unbalance between devices. Paralleling helps to reduce conduction losses and junction to case thermal resistance.

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SUMMARY:

- General guidelines
- Steady state sharing
- Dynamic sharing at turn-on
- Dynamic sharing at turn-off
- Related topics

Whenever devices are operated in parallel, due consideration should be given to the sharing between devices to ensure that the individual units are operated within their limits. Items that must be considered to successfully parallel MOSFETs are: gate circuitry, layout considerations, current unbalance, and temperature unbalance between devices. Paralleling helps to reduce conduction losses and junction to case thermal resistance. However, switching losses remain the same, or may even increase. If they are the dominant losses, only a thermal resistance improvement will be achieved by paralleling. Paralleling to take advantage of lower price of smaller devices should not be attempted without due consideration of the technical risks. Experimental results should be obtained at the extremes of the manufacturing tolerances.

The three most important parameters from this point of view are: voltage, current, and junction temperature. Voltage unbalances will be briefly examined in a qualitative way in the next section with other general considerations. The effects of current and temperature unbalances will be analyzed in the following sections.

1. GENERAL GUIDELINES ON PARALLELING

Generally speaking, voltage equality isensured by the fact that the devices arein parallel. However, under transient conditions, voltage differentials canappear across devices, due to dI/dt effects in unequalized stray inductances.

The stray inductances of a typical power circuit, like the one shown in figure 1, have different effects, depending on where they are situated. The effects of the emitter and collector inductances that are common to the paralleled pair have been analyzed in INT-936 and will be ignored here.

An unbalance of 10 % in the stray inductances that are in series with each collector, combined with a dI/dt unbalance of 10 % translates in an unbalance of 20 % in the overshoot seen at turn-off (81 V vs. 121 V). To minimize these differentials both dI/dt's and stray inductances have to be matched. However, if the overshoot does not violate the ratings of the MOSFET, the differential in the turn-off losses is negligible.

The impact of the common emitter inductance on switching energy, on the other hand, is far from negligible, as explained in INT-937. Furthermore, the MOSFET with lower common source inductance turns off before the other, which is left to shoulder the entire load current during the turn-off transient. It follows that switchmode operation of paralleled IGBTs should not be undertaken unless the common emitter inductances are matched in value.

Figure 2 shows that when using paralleled devices, a low impedance path is generated that may be prone to parasitic self oscillations. This is analyzed in greater detail in ref. [1]. Individual gate resistors provide the necessary damping and gate decoupling to prevent oscillations.

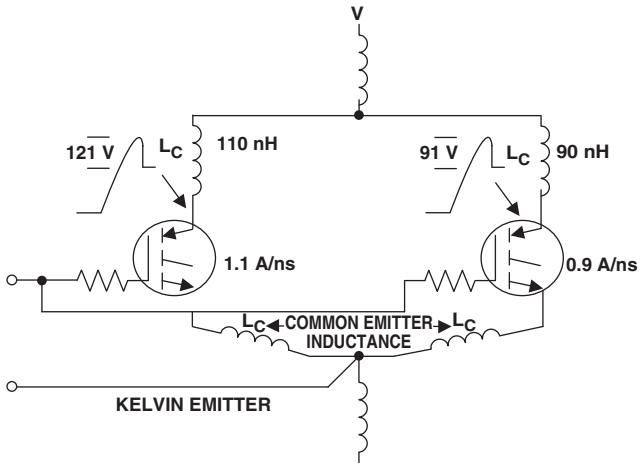

Fig. 1 - The effect of different dI/dt and stray inductances on collector

In summary, the following general guidelines should be followed when paralleling MOSFETs:

- Use individual gate resistors to eliminate the risk of parasitic oscillation;
- Equalize common emitter inductance and reduce it to a value that does not greatly impact the total switching losses at the frequency of operation;
- Reduce stray inductance to values that give acceptable overshoots at the maximum operating current.
- Ensure the gate of the MOSFET is looking into a stiff (voltage) source with as little impedance as practical. This advice applies equally well to both paralleled and single device designs.
- Zener diodes in gate drive circuits may cause oscillations. Do not place them directly gate to emitter/source to control gate overvoltage, instead place them on the driver side of the gate isolation resistor(s), if required.
- Capacitors in gate drive circuits may also cause oscillations. Do not place them directly gate to emitter/source to control switching times, instead increase the gate isolation resistor. Capacitors slow down switching, there by increasing the switching unbalance between devices.

Stray components are minimized by a tight layout and equalized by symmetrical position of components and routing of connections.

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These guidelines ensure that the voltage and switching unbalances due to the layout are negligible with respect to those due to the MOSFETs themselves, analyzed in the next sections.

Two questions must be considered: (1) “steady-state” sharing of current, and (2) dynamic sharing of current under the transitional switching conditions.

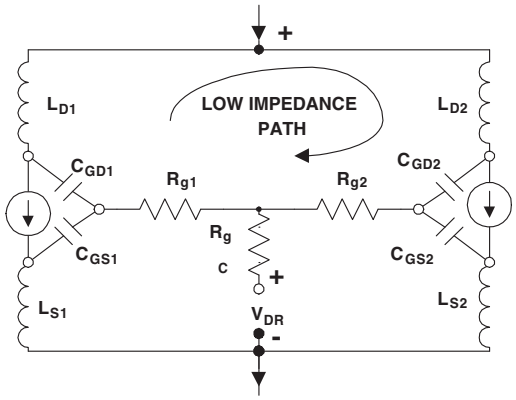

Fig. 2 - Low impedance Path for Parasitic Oscillation for Unbalanced Parallel Branches

2. STEADY-STATE SHARING OF CURRENT

During the periods outside of the switching transitions, the current in a parallel group of Power MOSFETs will distribute itself in the individual devices in inverse proportion to their on-resistance. The device with the lowest on-resistance will carry the highest current. This will, to an extent, be self-compensating, because the power loss in this device will be the highest. It will run hottest, and the increase in on-resistance due to heating will bemore than that of the other devices, which will tend to equalize the current.

An analysis of the “worst case” device current in a group of “N” parallel connected devices can be based on the simplifying assumption that (N - 1) devices have the highest limiting value of on-resistance, while just one lone device has the lowest limiting value of on-resistance. The analysis can then be concentrated on the current in this one device.

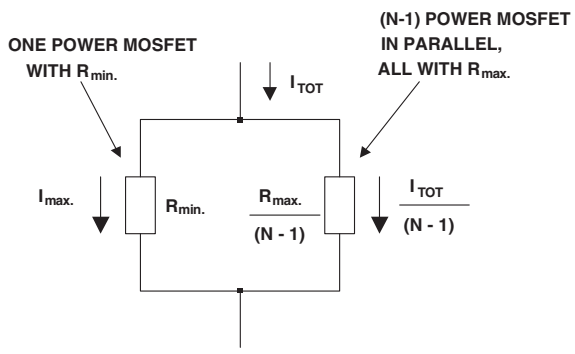

Fig. 3 - Simplified Equivalent Circuit for Estimating Worst Case Steady-State Current Unbalance

The equivalent electrical circuit shown in figure 3 simplifies the analysis further by assuming the number of devices is sufficiently large that the current that flows through each of the high resistance devices is approximately $I_{TOT}/(N - 1)$. On this assumption, the voltage drop across the lone low resistance device, and hence the current in it, can be calculated.

The on-resistance of each of the “high resistance” devices, at operating temperature, T, is given by:

$$R_{(max.)T} = R_{(max.)25}\left(1 + \left[(T_A - 25) + \frac{I^2_{TOT}}{(N - 1)^2} R_{(max.)T} R_{JA}\right]K\right) \quad (1)$$

where $R_{(max.)25}$ is the limiting maximum value of on-resistance at 25° C, R_{JA} is the total junction-to-ambient thermal resistance in °C/ W, and K is the per unit change of on-resistance per °C.

$$R_{(max.)T} = \frac{R_{(max.)25}(1 + [T_A - 25]K)}{1 - R_{(max.)25}\dfrac{I^2_{TOT}}{(N - 1)^2}R_{JA}K} \quad (2)$$

The voltage drop, V, across the parallel group is:

$$V = \frac{I_{TOT}}{(N - 1)} \times R_{JA}K \quad (3)$$

The resistance of the one low resistance device at its operating temperature is:

$$R_{(min.)T} = R_{(min.)25}(1 + [(T_A - 25) + V\, I_{(max.)}R_{JA}]K) \quad (4)$$

where $R_{(min.)25}$ is the limiting minimum value of on-resistance at 25 °C, and $I_{(max.)}$ is the current in this device.
But,

$$R_{(min.)T} = \frac{V}{I_{(max.)}}$$

$$\therefore I_{(max.)} = \frac{-b + \sqrt{b^2 + 4aV}}{2a} \quad (5)$$

where:
$b = R_{(min.)25}\,(1 + [T_A - 25]\,K)$
$a = R_{(min.)25}\,V\,R_{JA}\,K$

The following example shows the “worst case” degree of current sharing that can be expected, by applying the above relationships to the IRFP150 Power MOSFET, and making the following assumptions:
$R_{(max.)25} = 0.045\ \Omega$
$R_{(min.)25} = 0.035\ \Omega$
$R_{JA} = 3$ °C/W

$$\frac{I_{TOT}}{(N - 1)} = 20\ A \quad (6)$$

$K = 0.006$ per °C
$T_A = 35$ °C

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Using the relationships (2), (3), and (5) above, it can be calculated that the "worst case" maximum value of device current is 27 A for the hypothetical situation where all devices but one have high limiting on-resistance, of 0.0452 Ω and carry 20 A each, where as the remaining one has low limiting on-resistance of 0.03 Ω.

3. DYNAMIC SHARING OF CURRENT DURING TURN-ON

It is necessary to take positive steps to ensure that the current is distributed properly between a group of parallel connected devices during the switching transition. Since the Power MOSFETs will not all have identical threshold and gain characteristics, some will tend to switch sooner than others, and attempt to take more than their share of the current. Adding to the problem is the fact that circuit inductance associated with each device may be different, and this will also contribute to unbalancing the current under switching conditions. Here we will provide a brief qualitative description of the different events that occur during a switching transition.

The problem will be introduced by considering the switching waveforms for a typical clamped inductive load. Figure 4 shows waveforms of drain current, drain-to-source voltage, and gate voltage during the turn-on interval. For reasons of clarity we have shown the applied drive pulse increasing at are latively slow rate.

At time, t_0, the drive pulse starts its rise. At t_1, it reaches the threshold voltage of the Power MOSFET, and the drain current starts to increase. At this point, two things happen which make the gate-source voltage waveform deviate from its original "path". First, inductance in series with the source which is common to the gate circuit develops an induced voltage, as a result of the increasing source current. This voltage counteracts the applied gate drive voltage and slows down the rate-of-rise of voltage appearing directly across the gate and source terminals; this, in turn, slows down the rate-of-rise of the source current. This is a negative feedback effect; increasing current in the source produces a counteractive voltage at the gate, which tends to resist the change of current.

The second factor that influences the gate-source voltage is the so called "Miller" effect. During the period t_1 to t_2, some voltage is dropped across circuit inductance in series with the drain, and the drain-source voltage starts to fall. The decreasing drain-source voltage is reflected across the drain-gate capacitance, pulling a discharge current through it, and increasing the effective capacitance load on the drive circuit. This, in turn, increases the voltage drop across the impedance of the drive circuit and decreases the rate-of-rise of voltage appearing between the gate and source terminals. This also is a negative feedback effect; increasing current in the drain results in a fall of drain-to-source voltage, which, in turn, slows down the rise of gate-source voltage and tends to resist the increase of drain current. These effects are illustrated diagrammatically in figure 5.

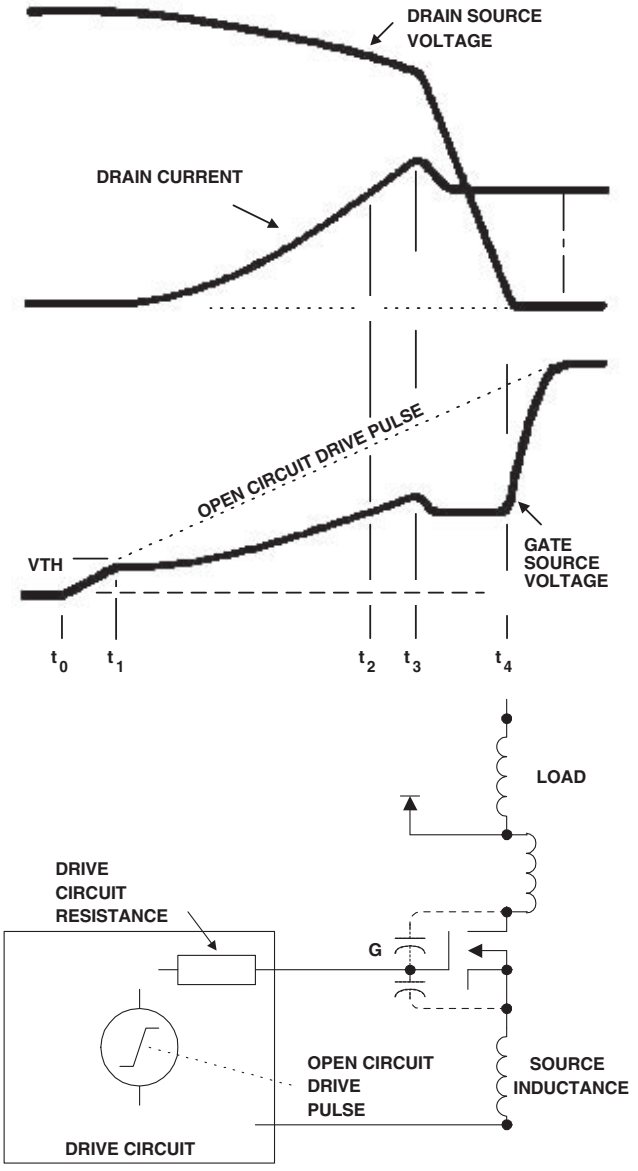

Fig. 4 - Waveforms at Turn-on

This state of affairs continues throughout the period t_1 to t_2, while the current in the Power MOSFET rises to the level of the current, I_M, already flowing in the freewheeling rectifier, and it continues into the next period, t_2 to t_3, while the current increases further, due to the reverse recovery of the freewheeling rectifier.

At time t_3, the freewheeling rectifier starts to support voltage, while the drain current and the drain voltage start to fall. The rate-of-fall of drain voltage is now governed by the Miller effect, and an equilibrium condition is reached, under

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which the drain voltage falls at just the rate necessary for the voltage between gate and source terminals to satisfy the level of drain current established by the load. This is why the gate-to-source voltage falls as there covery current of the freewheeling rectifier falls, then stays constant at a level corresponding to the motor current, while the drain voltage is falling.

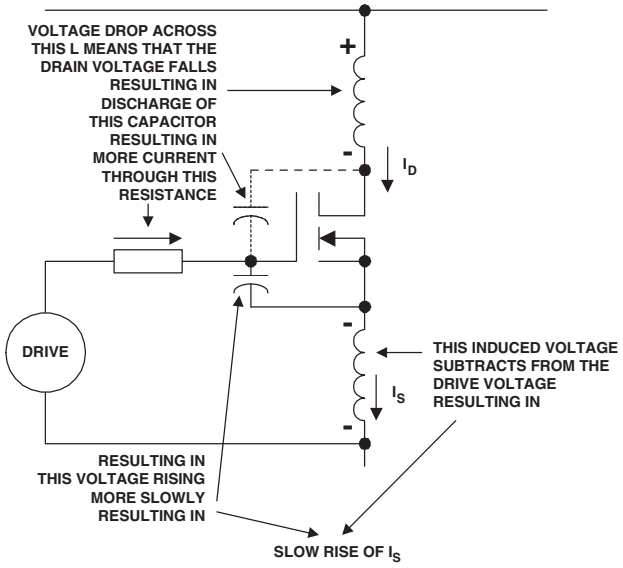


Fig. 5 - Diagrammatic Representation of Effects when Switching-ON

Finally, at time t_4, the Power MOSFET is switched fully on, and the gate-to-source voltage rises rapidly towards the applied “open circuit” value.

The above explanation, summarized in figure 5, provides the clue to the difficulties that can be expected with parallel connected devices. The first potential difficulty is that if we apply a common drive signal to all gates in a parallel group, then the first device to turn on - the one with the lowest threshold voltage - will tend to slow the rise of voltage on the gates of the others, and further delay the turn-on of these devices. This will be due to the Miller effect. The inductive feedback effect, on the other hand, only influences the gate voltage of its own device (assuming that each source has its own separate inductance). The second potential difficulty is that if the individual source inductances are unequal, then this will result in dynamic unbalance of current, even if the devices themselves are perfectly matched. Obviously, the solution to this is to ensure that inductances associated with the individual devices are as nearly equal as possible. This can be done by proper attention to the circuit layout.

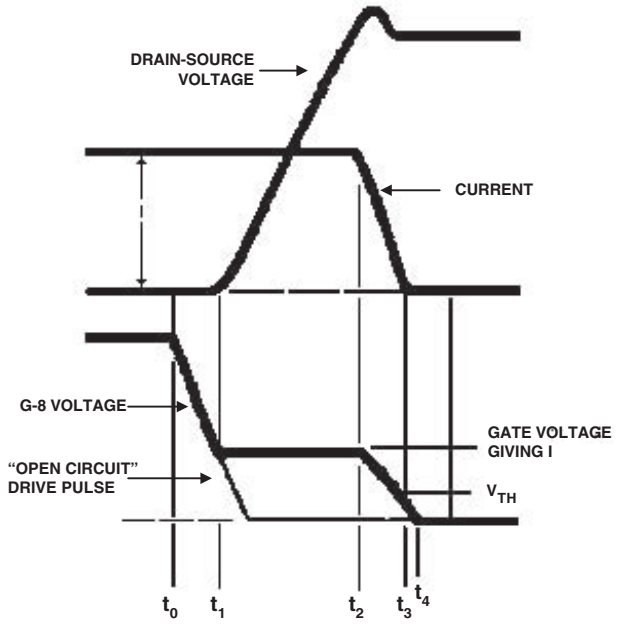
As examined in detail in ref. [1], there are several other circuit and device parameters that will contribute to dynamic unbalance. The conclusions presented in the above mentioned paper indicate, however, that the problem is not severe, as long as attention is paid to the following points, in order to ensure satisfactory sharing of current between parallel Power MOSFETs at turn-on:

- Threshold voltages should be within determined limits.
- Stray inductances throughout the circuit should be equalized by careful layout.
- Gates should be decoupled with individual resistors, but not more than strictly required, as it will be explained later.

4. DYNAMIC SHARING DURING TURN-OFF

Similar considerations apply to the dynamic sharing of current during the turn-off interval. Figure 6 shows theoretical waveforms for the circuit of figure 4 and 5 during the turn-off interval. At t_0, the gate drive starts to fall. At t_1, the gate voltage reaches a level that just sustains the drain current, I. The drain-to-source voltage now starts to rise. The Millereffect governs the rate-of-rise of drain voltage and holds the gate-to-source voltage at a level corresponding to the constantdrain current. At t_3, the rise of drain voltage is complete, and the gate voltage starts to fall at a rate determined by the gate-source circuit impedance, while the drain current falls to zero.

Figure 7 shows theoretical waveforms for two parallel connected Power MOSFETs with theirgates connected directly together. For purposes ofdiscussion, the source inductance is assumed to be zero. At t_1, the gate voltage reaches the point atwhich Power MOSFET B can no longer sustain its drain current.



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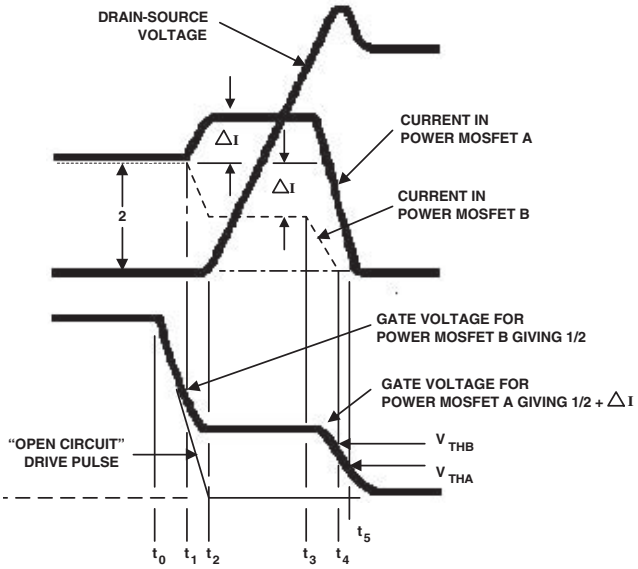

Fig. 6 - Waveforms at Turn-off

The load current now redistributes; current in Power MOSFET B decreases, while that in Power MOSFET A increases. At t_2, Power MOSFET B can no longer sustain its current; both Power MOSFETs now operate in their "linear" region, and the drain voltage starts to rise. The gate-to-source voltage is kept practically constant by the Miller effect, while the currents in the two Power MOSFETs remain at their separate levels. Clearly, the unbalance of current in this example is significant.

While a turn-off unbalance is potentially a more serious problem, the analysis in ref. [1] shows that this is not so in practice as long as the devices are turned off with a "hard" (very low impedance) gate drive. This by itself will almost guarantee limited dynamic unbalance at turn-off.

In summary, to achieve good sharing at turn-off the same precautions should be used as for turn-on, with the addition of a "hard" drive.

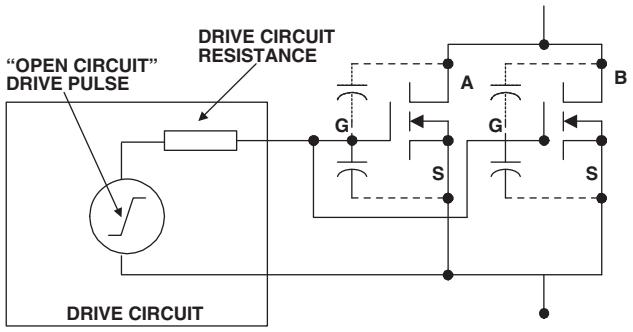

Fig. 7 - Waveforms at Turn-off - Two Power MOSFETs with Common Gates and Common Sources

References:

[1] J.B. Forsythe: "Paralleling of Power MOSFETs." IEEE-IAS Conference Record, October 1981.

Related topics:

- Gate drive requirements
- Thermal design
- Paralleling of IGBTs

APPLICATION NOTE